PVP 14

Code: EC5T3

III B.Tech - I Semester – Regular/Supplementary Examinations
October 2017

COMPUTER ARCHITECTURE AND ORGANIZATION
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) What is the role of multiplexers in a common bus system.
b) With an example, define Instruction Code.
c) What is a micro program?
d) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated?
e) What is meant by Handshaking in Data transfer communications?
f) How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes?
g) Why normalization is done in floating point representation?
h) Perform binary division of A(divisor) : 1011 and B(dividend) : 10100011 and write down the Quotient and Remainder.
i) What is parallel processing?

j) Define vector Processing.

k) Write any 2 applications of parallel processing.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2.a) If R1, R2 are source registers and R3 is destination register. Write down the logical Micro-operations for the following:

i) Ex-Or 2 M

ii) Ex-Nor 2 M

iii) AND 2 M

iv) OR 2 M

b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory, the instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

i) How many bits are there in the operation code, the register code part and the address part. 4 M

ii) How many bits are there in the data and address inputs of the memory. 4 M

3.a) Explain about Design of a control unit. 8 M

b) Briefly explain about Addressing modes. 8 M

4.a) What is DMA? Explain the terms Bus request, Bus grant in DMA. 8 M

b) Draw the block diagram of DMA controller and explain its working in brief. 8 M

5.a) Design an array multiplier for multiplying A(2bits) and B(2bits). 6 M

b) Draw the internal diagram of a BCD adder and explain its working. 10 M

6.a) What is pipeline? 4 M

b) Explain four segment instruction pipeline. 8 M

c) Name any two difficulties that cause the instruction pipeline to deviate from its normal operation. 4 M